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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/896,975	06/29/2001	David Allen Crutchfield	2001-0445	9938

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EXAMINER	
MEEK, JACOB M	

ART UNIT	PAPER NUMBER
2637	

DATE MAILED: 06/08/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/896,975	CRUTCHFIELD ET AL.	
	Examiner	Art Unit	
	Jacob Meek	2637	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 February 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1 - 32* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1 - 32* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *22 February 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

1. Applicant's amendment filed on February 4, 2005 has been entered.

Drawings

2. The drawings were received on February 4, 2005. These drawings are acceptable.

Specification

3. The amendment was received on February 4, 2005. This amendment is acceptable.

Response to Arguments

4. Applicant's arguments with respect to provisional double patenting rejection of claims 1 – 5, 10, 11, 16 – 19, and 28 – 32 have been considered but are not persuasive. The additional limitation of detecting and adjusting a communication rate is not a patentably distinct limitation, as it is well known in the art. The claimed support for differing communications standards also does not render the claimed invention unique, as a communications device could be readily adapted to any communication standard.

5. Applicant's arguments with respect to claims 1 - 32 have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 1 – 19, and 22 – 32 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ryan (US 6,359,946).

With regard to claim 1, Ryan discloses a method for effecting synchronous pulse generation for use in variable speed serial communications, comprising the steps of: obtaining a communication link speed (see column 9, lines 38 – 47 where this is interpreted as equivalent); providing a clock signal (see column 9, lines 27 – 30), providing a counter (see figure 5, 60 and column 9, lines 24 – 30), defining a sample count value of counter using communication link speed (see column 9, lines 30 – 33 where this is interpreted as equivalent), incrementing counter in relation to clock signal, determining whether current count value of counter corresponds to sample count value, and if current count value corresponds to sample count value then performing a step of generating a synchronous pulse (see column 9, lines 33 – 41), and if current count value does not correspond to sample count value then performing a step of determining whether a signal level has changed, and if difference signal has changed then performing a step of ignoring further changes in signal level of difference signal until current count value of counter corresponds to sample count value at which time step of generating synchronous pulse is repeated (see column 9, line 66 – column 10, line 8). Ryan is silent with respect to "difference signal." Ryan does teach a method of receiving serial communications of which differential signals are one of a known technique for the transmission of serial data and therefore would be a design choice according to system application.

With regard to claim 2, Ryan teaches a method wherein synchronous pulse is used to signify a time for performing a step of sampling difference signal to extract data from difference signal (see figure 1, SCLK, data signal, 200 and column 13, lines 22 – 25).

With regard to claim 3, Ryan teaches a method further comprising a step of defining a maximum count value of counter wherein if current count value corresponds to maximum count value then performing a step of resetting counter (see column 9, lines 33 – 41).

With regard to claim 4, Ryan teaches a method of determining whether signal level of difference signal has changed comprises the steps of: checking signal level of difference signal each cycle of clock signal (see figure 3), storing signal level of difference signal at a 1st clock cycle as a temporary signal difference signal (see figure 3, 40 Q), checking signal level at a 2nd clock cycle (see figure 3, CLK where oscillator continuously samples difference signal), checking signal level of difference signal at a 2nd clock cycle (see figure 3, CLK where oscillator continuously samples difference signal), and comparing signal level of temporary difference signal with signal level of difference signal at 2nd clock cycle (see figure 3, data signal, Q CLK where oscillator continuously samples difference signal).

With regard to claim 5, Ryan teaches a method wherein step of ignoring further changes in signal level of difference signal further comprises the steps of: resetting counter (see column 10, lines 26 – 29), determining whether current count value corresponds to sample count value; and if current count value does not correspond to sample count value the performing step of incrementing counter each clock cycle until current count value corresponds to sample count value at which time a step of sampling difference signal to extract data from difference signal is performed (see column 9, lines 33 – 41).

With regard to claim 6 - 9, Ryan is silent with respect to IEEE – 1394b communications link speeds. Ryan teaches a serial communications receiver capable of various data rates

and types (see column 9, lines 41 – 47). IEEE – 1394b is a known serial communications data standard and therefore would have been obvious to one of ordinary art to adapt Ryan's serial communications receiver to support communication link speeds as defined in IEEE – 1394b communications standards.

With regard to claim 10, Ryan discloses a method of extracting data, comprising the steps of: providing a clock signal (see column 9, lines 27 – 30), determining a communication link speed (see column 4, lines 48 – 52 where this is interpreted as equivalent); providing a counter (see figure 5, 60 and column 9, lines 24 – 30), defining a sample count value of counter utilizing communication link speed (see column 9, lines 30 – 33), incrementing counter in relation to clock signal, determining whether current count value of counter corresponds to sample count value, and if current count value corresponds to sample count value then performing a step of generating a synchronous pulse (see column 9, lines 33 – 41), and if current count value does not correspond to sample count value then performing a step of determining whether a signal level has changed, and if difference signal has changed then performing a step of ignoring further changes in signal level of difference signal until current count value of counter corresponds to sample count value at which time step of generating synchronous pulse is repeated (see column 9, line 66 – column 10, line 8). Ryan is silent with respect to "difference signal." Ryan does teach a method of receiving serial communications of which differential signals are one of a known technique for the transmission of serial data and therefore would be a design choice according to system application.

With regard to claim 11, Ryan teaches a method wherein current count value corresponds to sample count value, method further comprises step of generating a

synchronization pulse to signify a time for sampling of difference signal to extract data from difference signal (see figure 5, SCLK, data signal, 200 and abstract).

With regard to claims 12 – 18, these claims are analyzed as claims 6 – 9, 3 – 5, respectively, above.

With regard to claim 19, Ryan teaches a variable speed communications device comprising; a synchronous pulse generator having a data signal input (see figure 5, data signal), a clock signal (see column 9, lines 27 – 30), a speed input (see column 9, lines 30 – 33 where this is interpreted as equivalent), and a synchronous pulse output (see figure 5, SCLK where this is interpreted as equivalent), speed input adapted to receive a variable representative of a communications link speed (see column 9, lines 30 – 33) and a data signal input being coupled to receive data signal and clock signal input adapted to receive a clock signal (see column 9, lines 27 – 30 where this is interpreted as equivalent), wherein synchronous pulse generator processes clock signal and data signal to generate as synchronous pulse used for extracting data using clock signal (see figure 5, and column 9, lines 27 – 33 where this is interpreted as equivalent), and sampling data signal when synchronous pulse is asserted (see column 13, lines23 – 26 where SCLK is interpreted as clocking signal output as a synchronous pulse). Ryan is silent with respect to "difference signal." Ryan does teach a method of receiving serial communications of which differential signals are one of a known technique for the transmission of serial data and therefore would be a design choice according to system application.

With regard to claim 22 and 23, Ryan teaches an apparatus wherein synchronous pulse generator comprises means for selecting between data rates (see column 9, lines 41 – 47 where this is interpreted as equivalent functionality). Ryan is silent with respect to IEEE-1394 communication bus speeds. Ryan teaches a serial communications receiver capable of

various data rates (see column 9, lines 41 – 47). IEEE-1394 is a known serial communications data standard and therefore would have been obvious to one of ordinary art to adapt Ryan's serial communications receiver to support IEEE-1394 standards.

With regard to claim 24, Ryan teaches a communications device comprising; ; a synchronous pulse generator having a data signal input (see figure 5, data signal), a clock signal (see column 9, lines 27 – 30), a speed input (see column 9, lines 30 – 33 where this is interpreted as equivalent), and a synchronous pulse output (see figure 5, SCLK where this is interpreted as equivalent), speed input adapted to receive a variable representative of a communications link speed (see column 9, lines 30 – 33) and a data signal input being coupled to receive data signal and clock signal input adapted to receive a clock signal (see column 9, lines 27 – 30 where this is interpreted as equivalent), wherein synchronous pulse generator processes clock signal and data signal to generate as synchronous pulse used for extracting data using clock signal (see figure 5, and column 9, lines 27 – 33 where this is interpreted as equivalent), and sampling data signal when synchronous pulse is asserted (see column 13, lines23 – 26 where SCLK is interpreted as clocking signal output as a synchronous pulse), a serial interface engine having a 2nd difference signal input, a synchronous pulse input, and a parallel output, and SIE processing serial data and outputting parallel data (see figure 5, 200, data signal, SCLK; figure 7, and column 13, lines 23 – 39 where this is interpreted as equivalent functionality). . Ryan is silent with respect to "difference signal", IEEE-1394b, 8b/10b decoder, and descrambler. Ryan discloses a method of receiving serial communications of which IEEE-1394b is a known standard utilizing differential signals for the transmission of serial data and therefore would have been obvious for an IEEE-1394b system application. IEEE-1394b, figure 10-2 clearly defines the requirements for an 8b/10b encoder and scrambler along with the needs for reciprocal

functions (page 141 last paragraph). It would have been obvious to one of ordinary skill in the art at the time of invention to provide support for IEEE-1394b in view of Ryan's disclosure of a device adaptable for various communications standards (see column 2, lines 37 – 42). The particular circuit naming convention as claimed by applicant is design choice.

With regard to claim 25, Ryan is silent on the use of connection manager having a toning input, a toning output and a bus speed output. IEEE 1394b specification defines the use of connection manager having a toning input, a toning output and a bus speed output (see section 6.6, 6,6,1). It would have been obvious to one of ordinary skill in the art at the time of invention to support an IEEE 1394b system in view of Ryan's disclosure of a device adaptable for various communications standards (see column 2, lines 37 – 42).

With regard to claims 26– 27, these claims are analyzed as claims 22 and 23 above.

With regard to claim 28, Ryan discloses a method for synchronizing a receiver to data, comprising the steps of: detecting a data speed (see column 4, lines 48 – 52), initializing a counter to count clock cycles (see column 9, lines 30 – 33 where loading of bit-rate value is interpreted as performing this function), detecting a current counter value (see column 9, lines 33 – 41), defining a sampling count value based on data speed (see figure 5, 60 and column 9, lines 24 – 30), detecting a change in data (see figure 3, edge), incrementing counter if no change in data is detected, generating a synchronous pulse when counter reaches sampling count value (see column 9, lines 33 – 41). Ryan is silent with sampling data with clock when pulse is asserted. Ryan does teach that SCLK (synchronous pulse) is derived from single clock. Using a combinatorial logic function of SCLK and system clock would be a design choice.

With regard to claim 29, Ryan teaches a method wherein generating step occurs if a change in data is detected (see column 10, lines 13 – 18).

With regard to claim 30, Ryan teaches a method wherein generating step occurs when count value equals sampling count value (see column 9, lines 33 – 41).

With regard to claim 31, Ryan teaches a method further comprising the step of delaying pulse to center pulse in a data bit (see column 11, lines 17 – 21 where this is interpreted as inclusive).

With regard to claim 32, Ryan teaches a counter where this is an inherent feature of a modulo-n counter.

7. Claims 20 - 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ryan (US 6,359,946) in view of IEEE-1394b, Draft 1.11.

With regard to claim 20, Ryan teaches a variable speed communications device further comprising a comprising a serial interface engine having a 2nd difference signal input, a synchronous pulse input, and a parallel output, and SIE processing serial data and outputting parallel data (see figure 5, 200, data signal, SCLK; figure 7, and column 13, lines 23 – 39 where this is interpreted as equivalent functionality). Ryan is silent with respect 8b/10b decoder, and descrambler. IEEE-1394b, figure 10-2 clearly defines the requirements for an 8b/10b encoder and scrambler along with the needs for reciprocal functions (page 141 last paragraph). It would have been obvious to one of ordinary skill in the art at the time of invention to provide support for IEEE-1394b in view of Ryan's disclosure of a device adaptable for various communications standards (see column 2, lines 37 – 42). The particular circuit naming convention as claimed by applicant is design choice.

With regard to claim 21, Ryan is silent with respect to a packet receiver / transmitter having a parallel input, parallel input coupled to parallel output of descrambler. IEEE-1394b, figure 4-1 clearly shows a packet receiver/transmitter, which connects to communication port incorporating other limitations. It would have been obvious to one of ordinary skill in the art

at the time of invention to provide support for IEEE-1394b in view of Ryan's disclosure of a device adaptable for various communications standards (see column 2, lines 37 – 42).

Other Cited Prior Art

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Schowe (US-3,938,082), Scarpa (US-5,444,743), and Brauns (US-5,689,533) all disclose apparatus for the alignment of clock and data. Gutz (US-5,072,407) and Earnest (US-5,982,837) disclose apparatus and techniques for the detection of data rates.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jacob Meek whose telephone number is (571)272-3013. The examiner can normally be reached on 8:00 - 4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jay Patel can be reached on (571)272-2988. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

JMM

JAY K. PATEL
SUPERVISORY PATENT EXAMINER